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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,222	01/14/2004	John David Kaewell JR.	I-1-0064.5US	3792

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VOLPE AND KOENIG, P.C.
DEPT. ICC
UNITED PLAZA, SUITE 1600
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103

EXAMINER	
CHEN, JUNPENG	
ART UNIT	**PAPER NUMBER**
2618	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,222	KAEWELL ET AL.	
	Examiner	Art Unit	
	JUNPENG CHEN	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-12,14-16,18-22,24-26,28-32,34-36 and 38-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12,14-16,18-22,24-26,28-32,34-36 and 38-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to applicant's amendment/arguments filed on 04/30/2010. Independent claims 9, 19 and 29 have been amended. Claims 52-54 have been added. Currently, claims 9-12, 14-16, 18-22, 24-26, 28-32, 34-36 and 38-54 are pending. **This action is made FINAL**.

Response to Arguments

2. Applicant's arguments filed 04/30/3010 have been fully considered but they are not persuasive.

Regarding claim 9, on pages 14 and 15 of the remark, applicant argues that "Ariyavisitakul teaches that the strength of the transmission power between the portable device and the fixed port is based on the three different parameters" and therefore "does not teach or suggest a third signal processing state having an intermediate power consumption level". The Examiner respectfully disagrees. Ariyavisitakul's system is a TDMA system, which inherently comprising the receiving time slot and the transmitting time slot. In the receiving time slot, the circuit elements in the transmitter are disabled (off power signal state signal processing state). In the transmitting slot, the circuit elements (i.e. at least the circuit elements of the power amplifier) are operating in at least two different power signal processing states as the power supplied to the circuit elements of the transmitter are different (i.e. high power signal processing state and intermediate power signal processing state) based on the dynamically adjustment

(up/down) of the supply power, Figure 3, col. 15 of line 56 to col. 16 of line 28. Therefore, Ariyavisitakul discloses the limitation in question, consequently, the rejection is maintained.

On page 15, applicant further argues that Ariyavisitakul's teaching is limited to a signal component, a transmitter. The Examiner would like to point out that the transmitter is a big component, however, as well-known in the art, the transmitter comprises more than one, or a plurality, of smaller circuit elements. Because the circuit elements of the transmitter are operating in different power signal processing states as discussed above, applicant's argument is considered non-persuasive.

Regarding claims 19 and 29, see response to claim 9 above.

Response to Amendment

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 9-12, 14-16, 18-22, 24-26, 28-32, 34-36 and 38-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al. (U.S. Patent 5,150,361) in view of **Ariyavisitakul** et al. (U.S. Patent 5,333,175).

Consider **claim 9**, Wieczorek discloses a time division multiple access (TDMA) wireless subscriber unit comprising:

a plurality of circuit components, wherein each of the plurality of circuit components is configured to operate in a first signal processing state having an on power consumption level, a second signal processing state having an off power consumption level (read as non-energy saving mode and the lower power mode, col. 5 with lines 4-21); and

a power interface circuit coupled to the plurality of circuit components: wherein the power interface circuit is configured to provide at least one of the on power consumption level, and the off power consumption level (read as battery saver 351 during non-energy saving mode and the lower power mode, Figure 3),

However, Wieczorek discloses the claimed invention above but does not specifically disclose a third signal processing state having an intermediate power consumption level, which couples to the power interface circuit, and wherein at least one of the plurality of circuit components is configured to transition among at least two of the first signal processing state, the second signal processing state and the third signal processing state, based on a time slot of a TDMA frame assigned to the TDMA wireless subscriber unit.

Nonetheless, in related art, Ariyavisitakui discloses a method and apparatus for dynamic power control in TDMA portable radio system, which inherently comprising the receiving time slot and the transmitting time slot. In the receiving time slot, the circuit elements in the transmitter are disabled (off power signal state signal processing state). In the transmitting slot, the circuit elements (i.e. at least the circuit elements of the power amplifier) are operating in at least two different power signal processing states as the power supplied to the circuit elements of the transmitter are different (i.e. high power signal processing state and intermediate power signal processing state) based on the dynamically adjustment (up/down) of the supply power, Figure 3, col. 15 of line 56 to col. 16 of line 28.

Therefore, it would have be obvious for a person with ordinary skill in the art at the time the invention was made to incorporate the teachings of Ariyavisitakul into the teachings of Wieczorek for reducing the power consumption by dynamically controlling the power usages.

Consider **claim 19**, Wieczorek discloses a method for use in a time division multiple access (TDMA) wireless subscriber unit, the method comprising: synchronizing phase with a received signal (read as the synchronization signal 310, controller 320 and synthesizer 334, Figure 3, col. 4 with lines 1-63); operating each a plurality of circuit components in a first signal processing state having an on power consumption level, a second signal processing state having an off power consumption level (read as non-energy saving mode and the lower power mode, col. 5 with lines 4-21),

transitioning at least one of the plurality of circuit components *among* the first signal processing state and the second signal processing state based on a time slot of a TDMA frame assigned to the TDMA wireless subscriber unit (read as the D/A 322, col. 4 with lines 24-27).

However, Wieczorek discloses the claimed invention above but does not specifically disclose a third signal processing state having an intermediate power consumption level, and wherein at least one of the plurality of circuit components is configured to transition among at least two of the first signal processing state, the second signal processing state and the third signal processing state, based on a time slot of a TDMA frame assigned to the TDMA wireless subscriber unit.

Nonetheless, in related art, Ariyavisitakui discloses a method and apparatus for dynamic power control in TDMA portable radio system, which inherently comprising the receiving time slot and the transmitting time slot. In the receiving time slot, the circuit elements in the transmitter are disabled (off power signal state signal processing state). In the transmitting slot, the circuit elements (i.e. at least the circuit elements of the power amplifier) are operating in at least two different power signal processing states as the power supplied to the circuit elements of the transmitter are different (i.e. high power signal processing state and intermediate power signal processing state) based on the dynamically adjustment (up/down) of the supply power, Figure 3, col. 15 of line 56 to col. 16 of line 28.

Therefore, it would have be obvious for a person with ordinary skill in the art at the time the invention was made to incorporate the teachings of Ariyavisitakul into the teachings of Wieczorek for reducing the power consumption by dynamically controlling the power usages.

Consider **claim 29**, Wieczorek discloses a processor comprising:

a power interface circuit configured to power a plurality of circuit components (read as battery saver 351 during non-energy saving mode and the lower power mode, Figure 3), wherein each circuit component of the plurality of circuit components is configured to operate in a first signal processing state having an on power consumption level and a second signal processing state having an off power consumption level (read as non-energy saving mode and the lower power mode, col. 5 with lines 4-21);

wherein at least one of the plurality of circuit components is configured to transition transitions among the of first signal processing state and the second signal processing state based on a time slot of a TDMA frame (read as the D/A 322, col. 4 with lines 24-27).

However, Wieczorek discloses the claimed invention above but does not specifically disclose a third signal processing state having an intermediate power consumption level, and wherein at least one of the plurality of circuit components is configured to transition among at least two of the first signal processing state, the second signal processing state and the third signal processing state, based on a time slot of a TDMA frame assigned to the TDMA wireless subscriber unit.

Nonetheless, in related art, Ariyavisitakui discloses a method and apparatus for dynamic power control in TDMA portable radio system, which inherently comprising the receiving time slot and the transmitting time slot. In the receiving time slot, the circuit elements in the transmitter are disabled (off power signal state signal processing state). In the transmitting slot, the circuit elements (i.e. at least the circuit elements of the power amplifier) are operating in at least two different power signal processing states as the power supplied to the circuit elements of the transmitter are different (i.e. high power signal processing state and intermediate power signal processing state) based on the dynamically adjustment (up/down) of the supply power, Figure 3, col. 15 of line 56 to col. 16 of line 28.

Therefore, it would have be obvious for a person with ordinary skill in the art at the time the invention was made to incorporate the teachings of Ariyavisitakul into the

teachings of Wieczorek for reducing the power consumption by dynamically controlling the power usages.

Consider **claims 10, 20 and 30, as applied to claims 9, 19 and 29 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses a plurality of clocks, wherein one of the plurality of clocks is selected for one of the plurality of circuit components based on a current one of the first signal processing state, the second signal processing state, and the third signal processing states (read as the various clock signals, including but not limited to a TDM frame clock, slot clock, and data symbol clock that also exist in the RF communication units in Figure 3, col. 2 with lines 60-57).

Consider **claims 11, 21 and 31, as applied to claim 10, 20 and 30 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses a software controlled register coupled to the plurality of circuit components, wherein the software controller register is configured to produce the plurality of clocks (read as controller 320 inherently having software in it to process instructions to operate the communication unit, Figure 3, col. 4 with 39-66).

Consider **claims, 12, 22 and 32, as applied to claims 9, 19 and 29 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses wherein each circuit components of the plurality of circuit components is further configured to operate in fourth signal processing state including a reduced power sub-state (read as plurality of power adjustment states of Ariyavisitakul, Figure 3, Figure 3, col. 15 of line 56 to col. 16 of line 28 of Ariyavisitakul).

Consider **claims 14, 24 and 34, as applied to claims 13, 23 and 33 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses wherein one of the plurality of circuit components is configured to retain operating state information to resume processing in response to a transition from the third signal processing state to the first signal processing states (read as the controller 320 maintains operating (reduce speed when necessary) during all modes/states, Figure 3, col. 4 with 39-66).

Consider **claims 15, 25 and 35, as applied to claims 9, 19 and 29 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses wherein at least one of the plurality of circuit components is configured to transition from the first signal processing state to either the second signal processing state or the third signal processing state (read transmitter 324 is deactivated unless the communication unit is transmitting, col. 4 with lines 24-30).

Consider **claims 16, 26 and 36, as applied to claims 9, 19 and 29 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses wherein the plurality of circuit components are configured to be selectively operate in any one of the first signal processing state, the second signal processing state, and the third signal processing state responsive to a radio control channel timeslot to determine the presence of call traffic or a traffic channel assigned to the TDMA wireless subscriber unit (read as the re-activation of the circuit in the receiving section, col. 4 with line 60 to col. 5 with line 49).

Consider **claims 18, 28 and 38, as applied to claims 9, 19 and 29 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses wherein one of the

plurality of circuit components is configured to transition *among* the first signal processing state, the second signal processing state, and the third signal processing state during a signal time slot (read as different power levels (adjustments) during transmitter slot, Figure 3, Figure 3, col. 15 of line 56 to col. 16 of line 28 of Ariyavisitakul).

Consider **claim 39, as applied to claim 29 above**, Wieczorek, as modified by Ariyavisitakul, discloses wherein at least one of the pluralities of circuit components is collocated with the processor (read as Figure 3).

Consider **claims 40, 44 and 48, as applied to claims 9, 19 and 29 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses wherein a first circuit component and a second circuit component of the plurality of circuit components are configured to operate concurrently in the first and third signal processing state (read as the clock signal generator and timer in controller 320 during power adjustments of the transmitter, Figure 3, col. 15 of line 56 to col. 16 of line 28 of Ariyavisitakul).

Consider **claims 41, 45 and 49, as applied to claims 40, 44 and 48 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses wherein a third circuit component of the plurality of circuit components is configured to operate in the second signal processing state concurrently with the first and second circuit component (read as the D/A 322, col. 4 with lines 24-27).

Consider **claims 42, 46 and 50, as applied to claims 9, 19 and 49 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses wherein a first circuit component and a second circuit component of the plurality of circuit components are

configured to operate concurrently in the second and third signal processing states, respectively (read as clock generator (at reduced speed) and D/A 322, col. 4 with lines 24-27).

Consider **claims 43, 47 and 51, as applied to claims 42, 46 and 50 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses wherein a third circuit component of the plurality of circuit components is configured to operate in the first signal processing state concurrently with the first and second circuit components (read as the timer, clock generator (at reduced speed) and D/A 322, col. 4 with lines 24-27).

Consider **claims 52-54, as applied to claims 9, 19 and 49 above respectively**, Wieczorek, as modified by Ariyavisitakul, discloses wherein the plurality of circuit components are configured to operate in a first set of signal processing states associated with a first operating state, and in a second set of signal processing states associated with a second operating state, wherein the first set of signal processing states and the second set of signal processing states are different (read as the high power signal processing state and intermediate power signal processing state based on the dynamically adjustment (up/down) of the supply power, Figure 3, col. 15 of line 56 to col. 16 of line 28).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

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P.O. Box 1450
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Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junpeng Chen whose telephone number is (571) 270-1112. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Junpeng Chen
J.C./jc

/Edward Urban/

Supervisory Patent Examiner, Art Unit 2618